AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory system comprising:

a plurality of memory devices coupled one to another in a chain, including a first memory device and a last memory device; and

a memory controller coupled to the first memory device in the chain, the memory controller ~~and~~ configured to output a memory access command ~~that is received by each of~~ to the first memory ~~devices~~ device in the chain, wherein the memory access command ~~and that~~ selects a set of two or more of the memory devices to be accessed.

2. (Original) The memory system of claim 1 wherein the memory access command is a memory read command that selects a set of the memory devices to be read by the memory controller;

3. (Original) The memory system of claim 1 wherein the memory access command is a memory write command that selects a set of the memory devices to store a sequence of write data values.

4. (Original) The memory system of claim 1 wherein the set of memory devices comprises fewer than all the memory devices in the chain.

5. (Currently Amended) The memory system of claim ~~1~~ 6 wherein each of the memory devices in the chain, except ~~a~~ the last memory device, comprises an output port coupled to an input port of another of the memory devices.

6. (Currently Amended) The memory system of claim ~~5~~ 1 wherein each of the memory devices in the chain comprises an input port, the input port of the ~~a~~ first memory device ~~in the chain comprises an input port~~ being coupled to the memory controller to receive the memory access command.

7. (Currently Amended) The memory system of claim ~~6~~ 5 wherein the memory controller is coupled to the input port of the first memory device in the chain via a point-to-point signaling path.

8. (Original) The memory system of claim 7 wherein the output port of each memory device in the chain, except the last memory device, is coupled to the input port of one other of the memory devices via a point-to-point signaling path.

9. (Original) The memory system of claim 5 wherein the last memory device comprises an output port coupled to an input port of the memory controller.

10. (Currently Amended) The memory system of claim 1 wherein each of the memory devices in the chain comprises an interface register having a buffer input and a buffer output, the buffer output of each of the memory devices, except ~~a~~ the last memory device in the chain, being coupled to the buffer input of one other memory device in the chain via a respective point-to-point signaling path.

11. (Original) The memory system of claim 10 wherein each of the memory devices in the chain comprises a clock signal receiver coupled to receive a clock signal and having an output coupled to a strobe input of the interface register.

12. (Original) The memory system of claim 11 wherein the interface register within each of the memory devices is configured to store a value present at the buffer input in synchronism with each rising edge transition of the clock signal.

13. (Original) The memory system of claim 12 wherein the interface register within each of the memory devices is further configured to store a value present at the buffer input in synchronism with each falling edge transition of the clock signal.

14. (Original) The memory system of claim 11 wherein the interface register within each of the memory devices is configured to store a value present at the buffer input in synchronism with each falling edge transition of the clock signal.

15. (Currently Amended) The memory system of claim 11 wherein each of the memory devices further comprises a clock output driver having an input coupled to an output of the clock receiver and wherein each of the memory devices except the last memory device has an output coupled to an input of the clock signal receiver ~~within another one of the~~ of a next memory ~~devices~~device.

16. (Currently Amended) The memory system of claim 10 wherein ~~the~~ an interface register comprises a first plurality of edge-triggered storage elements each having a strobe input coupled to receive a clock signal.

17. (Currently Amended) The memory system of claim 16 wherein ~~the~~ an interface register further comprises a second plurality of edge-triggered storage elements each having a strobe input coupled to receive a complement of the clock signal.

18. (Currently Amended) The memory system of claim 14 wherein each of the memory devices in the chain further comprises an output data buffer and a select circuit, the select circuit having a first input port coupled to the output data buffer, a second input port coupled to the interface register and, in each of the memory devices in the chain except the last memory device, an output port coupled to the buffer input of the interface register of ~~the one other~~ a next memory device.

19. (Original) The memory system of claim 1 wherein each of the plurality of memory devices is a discrete integrated circuit device.

20. (Original) The memory system of claim 1 further comprising a substrate and wherein at least a portion of the memory devices are mounted to the substrate.

21. (Original) The memory system of claim 20 further comprising sets of conductive traces formed on the substrate and coupled between respective pairs of the memory devices mounted on the substrate.

22. (Original) The memory system of claim 1 further comprising a substrate having first and second surfaces, and wherein a first portion of the memory devices are mounted on the first surface of the substrate, and a second portion of the memory devices are mounted on the second surface of the substrate.

23. (Original) The memory system of claim 22 further comprising:

a first sets of conductive traces coupled between respective pairs of the memory devices mounted on the first surface of the substrate; and

a second sets of conductive traces coupled between respective pairs of the memory devices mounted on the second surface of the substrate.

24. (Original) The memory system of claim 23 further comprising a set of conductive traces extending from one of the memory devices mounted on the first surface to one of the memory devices mounted on the second surface.

25. (Original) The memory system of claim 22 further comprising an interconnection structure coupled to the memory controller, the substrate being removably coupled to the interconnection structure.

26. (Currently Amended) A method of operation in a memory controller, the method comprising:

receiving a memory access request ~~that specifies a range of memory addresses~~; and

outputting a memory access command to a plurality of memory devices coupled one to another in a chain, the memory access ~~request~~ command including selection information~~, based on the specified range of memory addresses, that selects a set of~~ to select two or more of the memory devices to be accessed.

27. (Original) The method of claim 26 wherein the memory devices in the chain are associated with respective memory identifiers, and wherein the selection information indicates at least two of the memory identifiers.

28. (Original) The method of claim 27 wherein each of the memory identifiers indicates a position, within the chain, of the associated memory device, and wherein the selection information comprises a start memory identifier and an end memory identifier that

collectively select all the memory devices disposed within the chain between the memory devices associated with the start and end memory identifiers.

29. (Original) The method of claim 28 wherein the start memory identifier and end memory identifier additionally select the two memory devices associated with the start and end memory identifiers.

30. (Original) The method of claim 26 wherein the memory access request is a read request and wherein the memory access command is a read command.

31. (Original) The method of claim 30 further comprising outputting a read-data pickup command to the plurality of memory devices after outputting the memory access command.

32. (Original) The method of claim 31 wherein outputting a read-data pickup command comprises outputting a read-data pickup command that includes the selection information that was included in the memory access command.

33. (Original) The method of claim 31 further comprising receiving read data from the set of the memory devices selected by the selection information.

34. (Original) The method of claim 31 wherein outputting a read-data pickup command after outputting the memory access command comprises delaying, after outputting the memory access command, for a predetermined number of cycles of a clock signal before outputting the read-data pickup command.

35. (Original) The method of claim 34 wherein delaying for the predetermined number of cycles of the clock signal comprises retrieving a delay value indicative of the predetermined number of cycles of the clock signal from a storage location within the memory controller.

36. (Original) The method of claim 35 wherein retrieving the delay value from the storage location comprises retrieving the delay value from one of a plurality of storage locations within the memory controller according to the set of the memory devices to be accessed.

37. (Original) The method of claim 36 further comprising reading parameter data from each of the memory devices in the chain during a configuration operation, generating the delay value based on the parameter data and storing the delay value in the one of the plurality of storage locations.

38. (Original) The method of claim 26 wherein the memory access request is a write request and wherein the memory access command is a write command.

39. (Original) The method of claim 38 further comprising:
receiving a plurality of write data values within the memory controller; and
outputting the plurality of write data values, one after another, to the plurality of memory devices.

40. (Currently Amended) The method of claim 39 wherein outputting the plurality of write data values to the plurality of memory devices ~~comprises outputting the plurality of write~~

~~data values after~~is performed subsequent to outputting the write command.

41. (Currently Amended) The method of claim 40 wherein outputting ~~the write command to the plurality of memory devices comprises outputting the write command to a first memory device in the chain via a point-to-point signaling path, and wherein outputting~~ the plurality of write data values ~~after outputting the write command~~ comprises outputting the plurality of write data values, one after another, to the first memory device via ~~the~~ a first point-to-point signaling path, and transmitting at least some of the write data values from the first memory device to a second memory device via a second point-to-point signaling path.

42. (Original) The method of claim 26 wherein outputting the memory access command to the plurality of memory devices coupled in a chain comprises outputting the memory access command to a first memory device in the chain, the first memory device being configured to receive the memory access command and retransmit the memory access command to a next-in-line memory device in the chain.

43. (Currently Amended) The method of claim 26 wherein receiving a memory access request ~~that~~ specifies ~~a range of~~an amount of memory ~~address comprises receiving a memory access request that specifies a starting address and a number of storage locations~~ to be accessed.

Claims 44-77 (Cancelled)